IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 7, July 2016

High Performance Column Level ADC for CMOS Imager using Switched Capacitor Technique

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Abstract: An integrating type analog to digital converter is commonly used to achieve a high resolution. In this work 12-bit Dual slope ADC is developed which is an integrating type ADC. To integrate the input signal it requires one integrator made up of one resistance in feed forward path and one feedback capacitance with opamp circuit. Switched capacitor based integrator is alternative technique to realize the integrating function. In this design resistance in feed forward is replaced with two switches and one capacitor. This technique requires non overlapping clock. One of the advantages of this technique is area minimization. This technique is easily compatible with technology. This dual slope column level ADC minimizes the conversion time. Two stage opamp is designed which has gain of 78.22 dB. This column level dual slope ADC is implemented using 180nm standard CMOS technology.

Keywords: ADC, CIS, CMOS, OPAMP.

I. INTRODUCTION

The requirement of CMOS image sensor is increasing day by day. This is due to expansion in mobile imaging, video imaging camera, optical sensors and industrial machine vision. This situation is expected to continue with increasing demands from emerging applications in biomedical imaging, remote sensing, digital surveillance, sensor networks and robotics etc [1]. The column level ADC that has an ADC in each column due to this it can achieve a good trade off among silicon surface area, frame rate, power consumption and fill factor, therefore column level ADC is most widely used [2]. Very large scale integration is attracting much attention due to increasing need of miniaturization. Nano scale integration is demand of current scenario [3]. Today portable devices have main concern in VLSI. It is due to limited power supply through battery. So, circuit should consume less power [4]. In recent times many digital imagers like digital single lens reflex, camcorders, built in cameras have been developed. However with this development in digital cameras the demand of higher pixel resolution has increased [5]. The pixel size has become a main interest to achieve a high resolution [6]. In CMOS image sensor applications, it is difficult to integrate the complex calibration circuits in limited channel pitch [7]. The architecture of ADC should have less number of transistors and it should be less complex in size. The integrating type ADC is adopted due to its good linearity and uniformity. It occupies less surface area on a small column pitch [8]. Interconnection of pixel array and column level ADC is depicted in fig.1.

Power and surface area reduction is important since they allow more number of channels on single chip. Technology scaling improves the digital performance.

Smaller surface area and higher conversion rate are direct benefits [9].

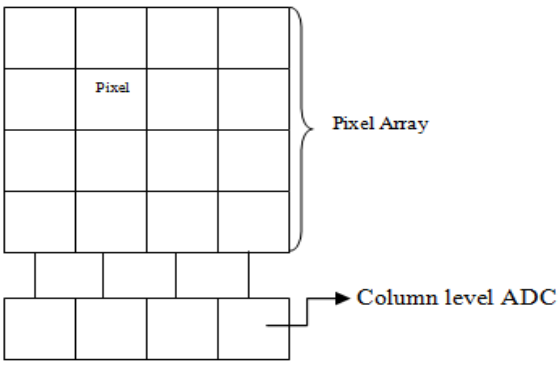

Fig.1 Pixel array with column level ADC

Surface area of the chip can also reduce with reducing the transistor's count [10]. Generally CIS comprises a pixel array, analog to digital converter and supporting digital blocks. Among them analog to digital converter converts the pixel voltage into digital code. Each pixel consists of one photodiode and some transistors. Photodiode is used to sense the light and transistor can act as reset, shutter and source follower [11]. Pixel converts light into electrical

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signal. This electrical output goes to analog to digital converter, then a significant amount of digital processing image enhancement and compression occurs [12]. The architecture of pixel may change according to application. Depending upon the application of device the circuit will change [13].The column level ADC have become popular because this have a large number of parallel ADC channels which provides high speed read out of large pixel arrays [14]. Popularity of these devices depends on small surface area, speed and reliability [15]. Scaling improves the transistor density on chip. It improves the frequency of operation and performance [16].

II. PROPOSED DUAL SLOPE ADC

Dual slope ADC is an integrating type ADC. It has high accuracy and linearity. So, it can be used as a column level ADC in CMOS image sensor. The dual slope ADC consists of integrator, comparator, counter and control logic. Generally integrator has one feed forward resistance and one feedback capacitance in RC technique. Resistance is depicted in equation 1.

$$R = \rho \frac{L}{A} (\Omega) \qquad (1)$$

Where R = resistance, ρ = resistivity, A = a plane perpendicular to the direction of current flow, L = Length.

Switched capacitor technique is used in this design replace this resistance with two switches and one capacitor. This technique is helpful in area reduction. This technique provides accuracy in time constant and easily compatible with technology. Two non-overlapping clock pulses are required for the operation of integrator. When a clock has a value of 1 during that time other clock must have the value of 0. It means there is no overlapping between these two clock pulses. Capacitance which emulates resistance is found out with equation2.

$$R = \frac{T}{C} \qquad (2)$$

Where R= Resistance, C= capacitance, T= Time period of clock pulse. This technique is very useful in area reduction. Schematic of dual slope ADC is shown in fig.2.

The conversion process of dual slope ADC is shown in fig.3.It is observed that the slope of the V_{int} is proportional to the amplitude of V_{in}^{*}. One reference voltage is given at the non inverting terminal of the integrator. Initially when switch1 is connected the integrator stabilizes itself at reference voltage. This reference voltage is provided at the non-inverting terminal of the integrator. At time t_0 switch1 is disconnected. At this time switch2 connects integrator's inverting terminal to signal voltage V_{in}^{*}.

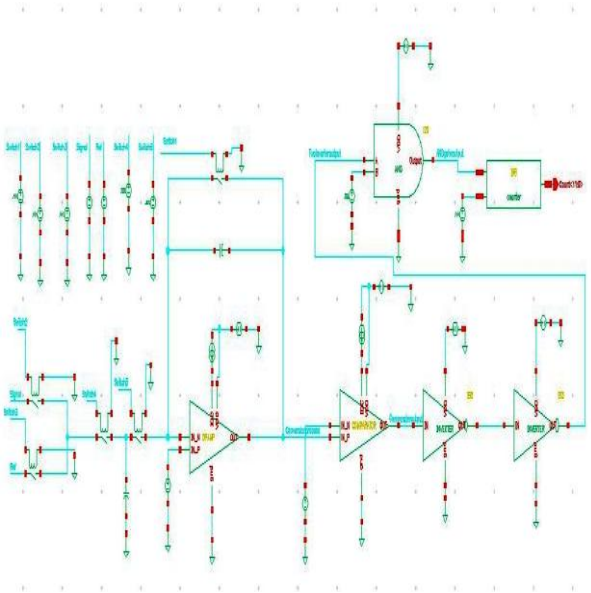

Fig.2 Full Schematic of Dual Slope ADC

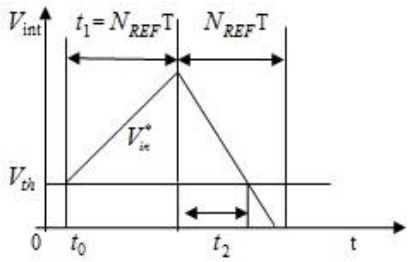

Fig.3 Waveform for Dual slope ADC

At this time capacitor starts charging and counter starts counting to particular time t_1, and then reset the counter. The voltage $V_{in}(t_1)$ at t = t_1.

$$V_{\text{int}}(t_1) = \text{K} \int_0^{N_{REF}T} V_{in}^{*} dt + V_{\text{int}}(0)$$

$$V_{\text{int}}(t_1) = \text{K} N_{REF}\,\text{T} V_{in}^{*} + V_{th} \qquad (3)$$

Where $t_1 = N_{REF}$ T and T = clock pulse.

At time t_1 Switch3 is connected to reference voltage V_{REF} and capacitor starts discharging. Counter again starts counting. When the output of the integrator reaches to the threshold voltage V_{th} of comparator, the counter will be stopped and binary count can be converted in to digital word N_{out}. t_2 is the time where the output of the integrator reaches to the V_{th} of comparator. The integrator voltage at $t_1 + t_2$ is given as

$$V_{\text{int}}(t_1 + t_2) = V_{\text{int}}(t_1) + \text{K} \int_{t_1}^{N_{out}T + t_1} (-V_{REF}) dt = V_{th} \qquad (4)$$

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Where $t_2 = T + t_1$
Substituting Eq. 3 in Eq. 4.

$$K N_{REF} T V_{in}^* + V_{th} - K V_{REF} N_{out} T = V_{th} \quad (5)$$

solving Eq. 5 for N_{out}

$$N_{out} = N_{REF} - \frac{V_{in}^*}{V_{REF}} \quad (6)$$

It has observed that N_{out} will be some fraction of N_{REF}, where fraction corresponds to the ratio of V_{in}^* to V_{REF} [17].

III. TWO- STAGE OPERATIONAL AMPLIFIER

Differential amplifier can be considered as the single stage operational amplifier. The two stage opamp is the combination of differential amplifier and common source amplifier. The schematic of two stage opamp is depicted in fig.4

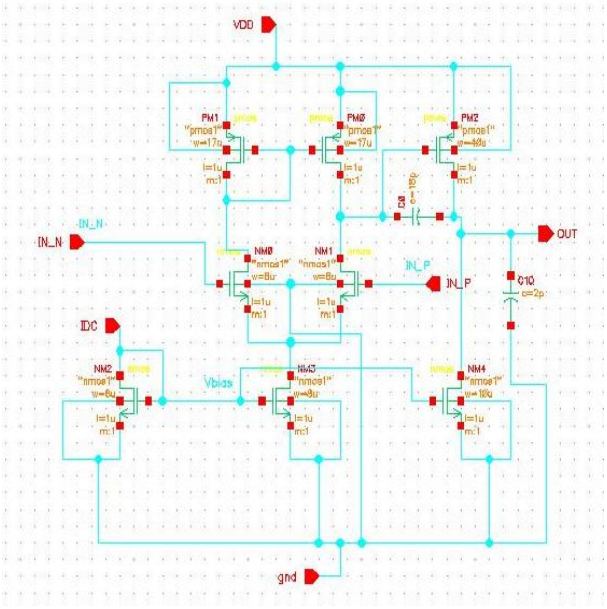

Fig.4 Schematic of Two stage Opamp

It is standard architecture with miller compensation technique applied in it. In two stage opamp first stage provides high gain and second stage provides large swings [18].

IV. RESULT AND DISCUSSIONS

Two stage opamp is very important block for dual slope ADC. Gain of two stage ADC is observed from the simulation which is 78.22 dB and unity gain bandwidth is 5MHz. It can see in AC analysis. Simulation for gain is depicted in fig.5

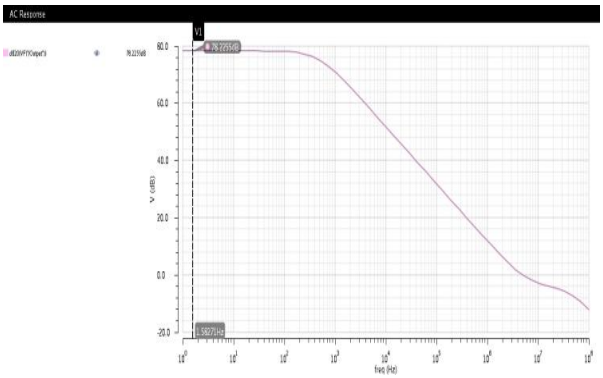

Fig.5 Gain of two stage Opamp

The phase margin of opamp is shown in fig.6 .It is about 44.81°.

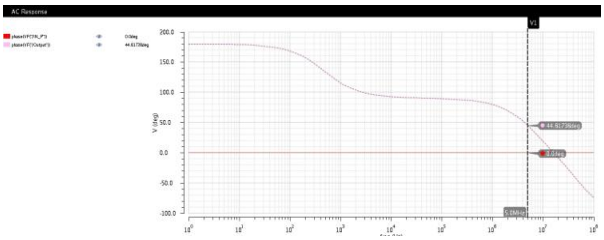

Fig6. Phase margin of two stage Opamp

DC analysis of two stage opamp is depicted in the fig.7. Same opamp has been used as comparator with miller capacitor removed and addition of inverter stages at output.

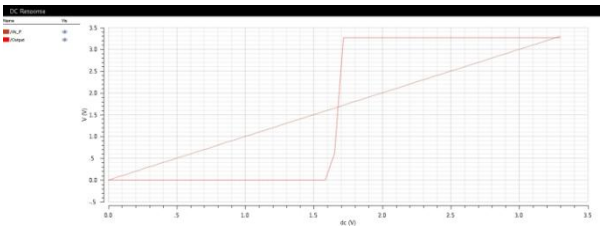

Fig.7 DC analysis of Two stage Opamp

It provides the value of input voltage where gain of opamp is high. Dual slope ADC using switched capacitor technique requires non overlapping clock pulses. The waveform of these pulses are shown in fig.8.

Fig. 8 Non- overlapping clock pulses

Simulation for proposed ADC is depicted in fig.9. It shows the operation of all the switches, non overlapping clock, conversion process, comparator output and AND gate output.

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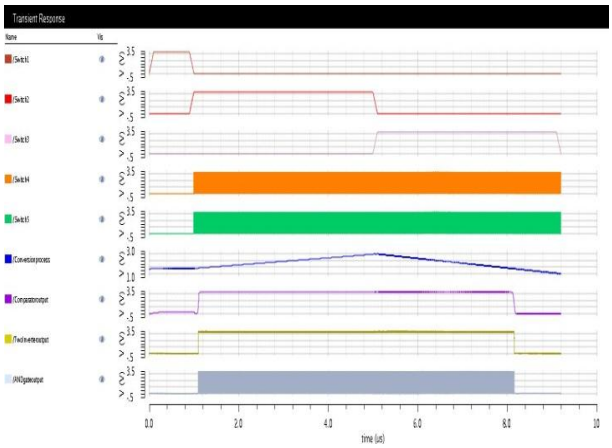

Fig.9 Simulation of dual slope ADC

Simulation of dual slope ADC shows the conversion time is 9.2µs. Simulation of 12-bit counter is shown in figure 10.

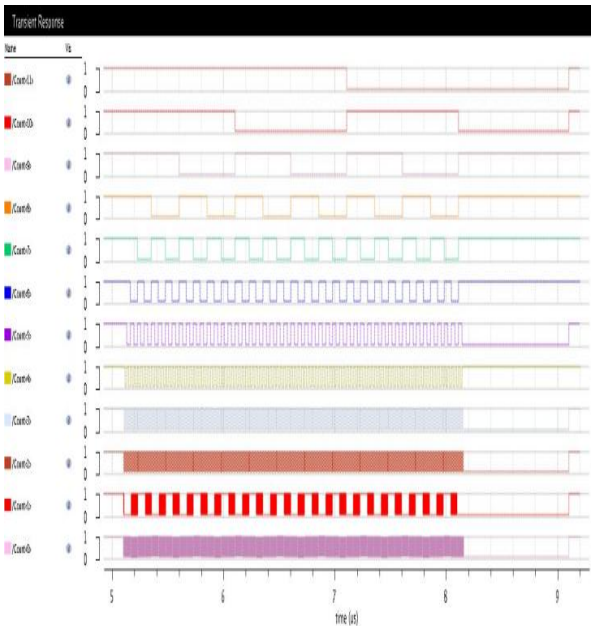

Fig.10 Simulation of 12-bit counter

When the integrator's output becomes equal to the threshold voltage of comparator counter stop counting and binary value converted in to digital form. The counter simulation is shown in the tabular form in table 1.

TABLE1. Simulation of 12-bit counter

Analog input	Reference Voltage	Threshold voltage of comparator	Dual slope ADC Output	Total Steps
V_{in}^{*} in volt	V_{REF} in volt	V_{th} in volt	12- bit	N_{out}
1.65	2.4	1.65	111111010100	4052
1.6	2.4	1.65	111010010011	3731
1.55	2.4	1.65	110101111111	3455
1.45	2.4	1.65	101101011000	2904
1.35	2.4	1.65	100100110001	2353
1.25	2.4	1.65	011100001010	1802
1.15	2.4	1.65	010011100011	1251
1.1	2.4	1.65	001111010000	976

The problem in counter's count, it can be solve by compensation methodology. It will improve in future work. Design summary of dual slope ADC along with opamp parameters is presented in Table 2.

TABLE2. Design summary of Dual slope ADC

Parameters	Proposed Work
Technology	0.18 µm
Type of ADC	Dual slope
Resolution	12 bit
Conversion time	9.2 µs
Opamp used	Two Stage
Gain of Opamp	78.22 dB
Phase margin of Opamp	44.81°
Opamp unity gain bandwidth	5MHz
Supply voltage	3.3 volt

The comparison of this dual slope ADC with architecture of ADC implemented in previous work is depicted in table3.

TABLE3. Comparison of parameters with other ADC

Parameters	[19]	[20]	Proposed Work
Technology	0.18µm	0.35 µm	0.18 µm
Type of ADC	SS/SAR	CDS-ADC	Dual slope
Resolution	11 bit	12 bit	12 bit
Conversion time	12 µs	41 µs	9.2 µs

It shows reduction of 23.33% in conversion time ADC of [19] while resolution is increased by 1bit and When compared with [20] conversion time reduces to 77.56% keeping resolution of both ADC same at 12-bit. Graphical representation of comparison is shown in fig.11.

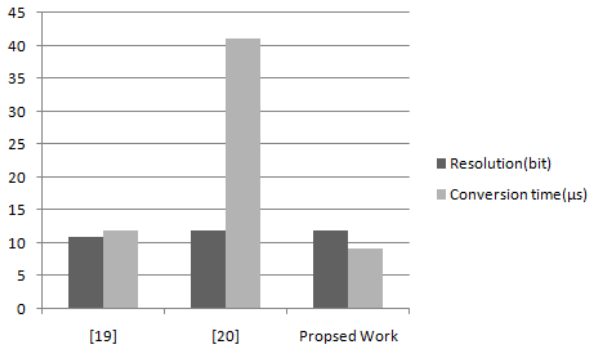

Fig.11 Graphical comparison of other ADC

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Tentative area prediction done for ADC:

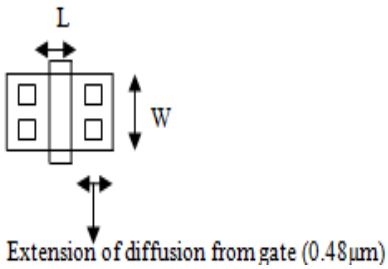

Fig.12 Layout of transistor

Total area of transistor in fig.12 is (L+2×0.48µm)×W. Calculate the all transistor's area in this way of the circuit and sum up all transistor's area of the circuit and then double the total area. This total area is the tentative area of that circuit. The total tentative area predicted of opamp is calculated from this way is 454.72 μm^2 .Layout density of standard cells in 180nm standard CMOS technology is 80Kgates / mm^2 .61 cells are required for counter. The tentative area prediction done for ADC without counter is 943.64 μm^2 . The power consumption of whole ADC is 3.7271mW.

V. CONCLUSION

Dual slope ADC is an integrating type ADC and is suitable for column level ADC for CMOS imager due to its high linearity. This proposed ADC has been designed using switched capacitor technique along with non overlapping clock pulses. Simulation result of dual slope column level ADC using switched capacitor technique shows the reduction of 23.33% in conversion time when there is increase of 1bit in resolution and reduction of 77.56% in conversion time for same resolution over the work previously carried out as depicted in table 3. Simulation results also show the binary count of 12-bit counter. This proposed ADC has two stage opamp having gain of 78.22 dB with unity gain bandwidth of 5MHz.Simulation of ADC is carried out using an 180nm standard CMOS technology.

ACKNOWLEDGEMENT

I would like to thank Mr. Anil koul (scientist/ Engineer 'SD'), VLSI Design Division, Semi-Conductor Laboratory, Mohali, India for his support and valuable guidance.

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Deep Sehgal Deep Sehgal is working as Scientist / Engineer in VLSI design in Semi-Conductor Laboratory, Department of Space, Government of India. Graduated from NIT (then REC) Surat, Gujarat in year 1996 in electronics stream; he joined SCL in year 1998. His dominant field of interest has been in analog design and all these years apart from working at levels of project member to project lead he has peer reviewed many designs and has been involved in testing and debugging of fabricated designs.

H.S. Jatana H.S. Jatana received B.Tech (Hons) from BITS Pilani in 1984 and joined CMC as software engineer, worked on Railway Computerization project for one year. Joined SCL in Oct 84. He has been involved in design of VLSI products, and have contributed in many design projects like range of transceivers (400Mbps to 1.2 Gbps), power management chips, converters (12-bit pipeline ADC, 12-bit current steering DAC, 16-bit sigma-delta), CMOS Imaging sensor, cold sparing pads, rad-hard tolerant digital cells and memory cell, and many ASICs. Has worked at Rockwell Semiconductor for design/characterization of R65 series of devices and at AMS Austria for porting of 2 um and 1.2 um CMOS processes and ATE testing/characterization of products fabricated in these processes. He specializes in analog CMOS design, characterization and ATE testing of VLSI chips.